35-BIT LED DISPLAY DRIVER

Part No: 80-08-00004

Type: PS035

FEATURES

— CMOS technology

— Continuous brightness control

— Serial data input

— No load signal required

— Optional external data enable and reset

— Wide power supply operation (3.5V to 10V)

— 34 or 35 outputs, 20mA sink capability

— Alphanumeric capability

APPLICATIONS

— Products with alphanumeric LED displays such as digital clock, counter, radio, multimeter, etc.

— Industrial control indicator or instrumentation readout

— Relay driver

ORDERING INFORMATION

PART NO.	TYPE NO.	PACKAGE	NOTE
80-08-00004	PS035	-	CHIP FORM

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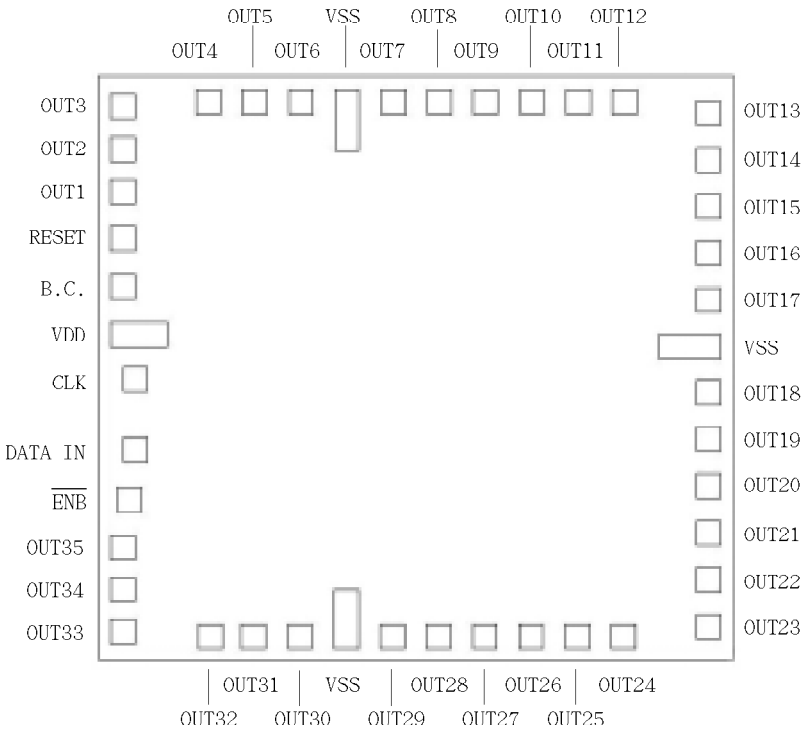
■ ABSOLUTE MAXIMUM RATINGS

Ta=+25℃, UNLESS OTHERWISE SPECIFIED			
CHARACTERISTICS	SYMBOL	RATING	UNIT
Supply Voltage	VDD	+3.5 ~ +10	V
Clock Frequency	FCLK	1M	Hz
Input Voltage	VIN	-0.3 ~ VDD+0.3	V
Input B.C. Current	IBC	700	μA
Output Sustaining Voltage	VDS	10	V
Output Continuous Current	IOUT	25	mA
Power Dissipation Per Output	PDISS	25	mW
Operating Temperature	TOPR	-40 ~ +85	℃
Storage Temperature	TSTR	-40 ~ +150	℃

■ PAD ASSIGNMENT (TOP VIEW)

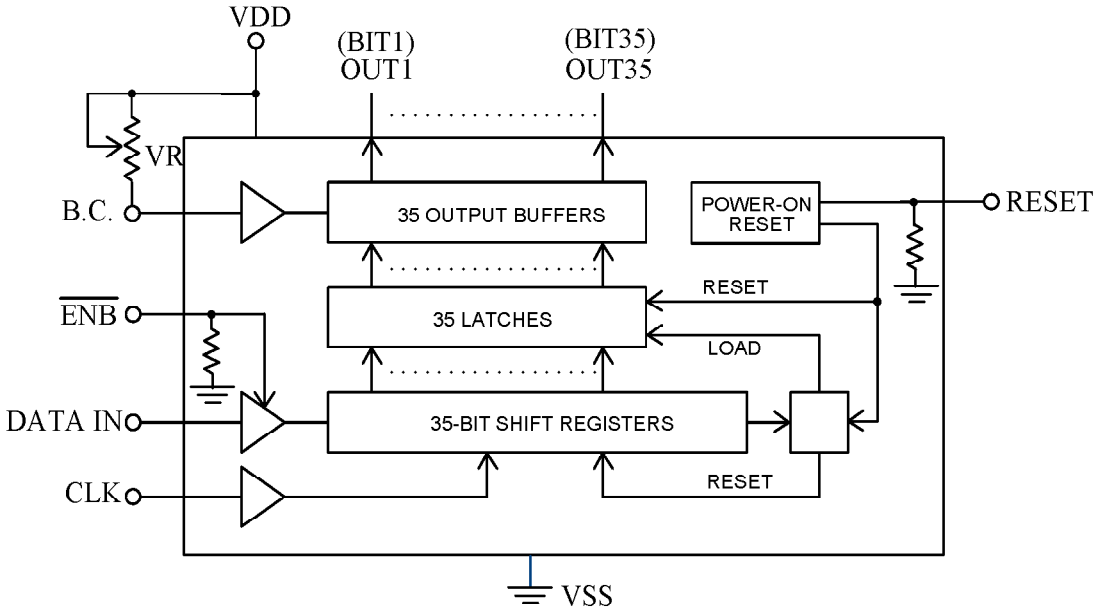


Die Size¡G2740um ¡Ñ2650um¡] W ¡ÑH¡^

¡½ PAD/PIN DESCRIPTIONS

PIN NO.	PIN/PAD NAME	TYPE	DESCRIPTION
16	VDD	Power	Power
6,28,39,40	VSS	Ground	Ground
–	RESET	Input	Reset signal input, (Normally grounded)
15	B.C.	Input	DC current input for LED brightness control
17	NC	–	No connection
18	CLK	Input	Clock input
19	DATA IN	Input	Serial data input
–	$\overline{ENB}$	Input	Data input enable, (Normally grounded)
1¯5;7¯14 20¯27;29¯38 41¯44	OUT1¯OUT35	Output	Open-drain NMOS output drivers

■ FUNCTION BLOCK DIAGRAM



¡½ FUNCTION DESCRIPTIONS

The PS035 is designed to drive either 4 or 5-digit, common anode alphanumeric LED displays with the added benefit of requiring minimal interface with the display or data source.

Data is transferred serially via 2 signals: clock and serial data. Data transfer without the added inconvenience of an external load signal is accomplished by using a format of a leading "1" followed by the allowed 35 data bits. These 35 data bits are latched after the 36th clock has been transferred. This scheme provides non-multiplexed, direct drive to the LED display. Characters currently displayed (thus, data output) changes only if the serial data bits differ from those previously transferred. Display brightness is determined by control of the output current for LED displays. This control function can be achieved by varying the current flowing into B.C. terminal. A simple way is to set an external variable resistor illustrated in the block diagram. Typically, the output current is 36 times greater that current into B.C. terminal.

Figure 1 shows the input data format. A leading "1" is followed by 35 bits of data. After the 36th had been transferred, a load signal is generated synchronously with the clock high state. This loads the 35 bits of data into the latches. A reset signal is generated consecutively with the clock low, which clears all shift registers for the next set of data. All shift registers are static master-slave, with no clear for the master portion of the first register, allowing continuous operation. There must be a complete 36 clocks or the shift registers will not clear.

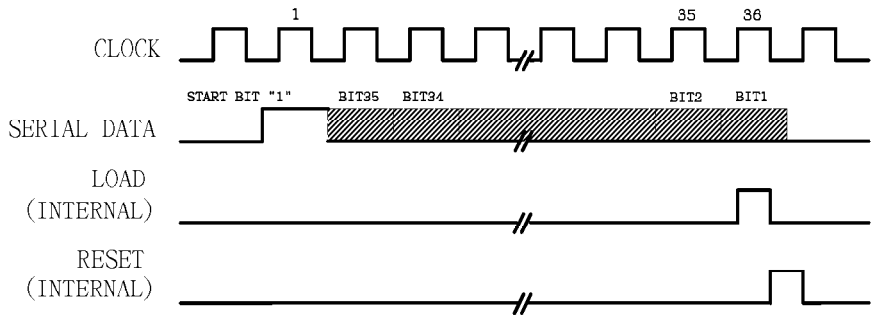
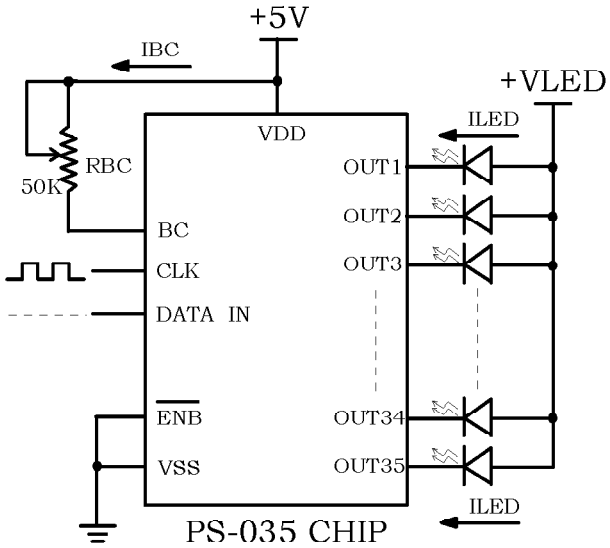


FIG.1 INPUT DATA FORMAT

When the chip first powers ON, a transient high state of internal power ON reset signal is generated which clears all shift registers and latches. The start bit and the first clock return the chip to its normal operation. The 'RESET' input terminal is also available for an option to clear all shift registers and latches by an external pulse.

■ TYPICAL APPLICATION CIRCUIT



IBC = (VDD—VBC) / RBC

ILED = 36 * IBC

■ RECOMMENDED OPERATING CONDITIONS

VDD=+5V, Ta=+25°C, UNLESS OTHERWISE SPECIFIED					
CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	VDD	4	5	9	V
Clock Frequency	FCLK	–	500K	2M	Hz
Input B.C. Current	IBC	0	–	550	μA
Output Sustaining Voltage	VDS	–	–	9	V
Output Continuous Current	IOUT	–	–	20	mA
Power Dissipation Per Output	PDISS	–	–	20	mW

ï½ DC ELECTRICAL CHARACTERISTICS

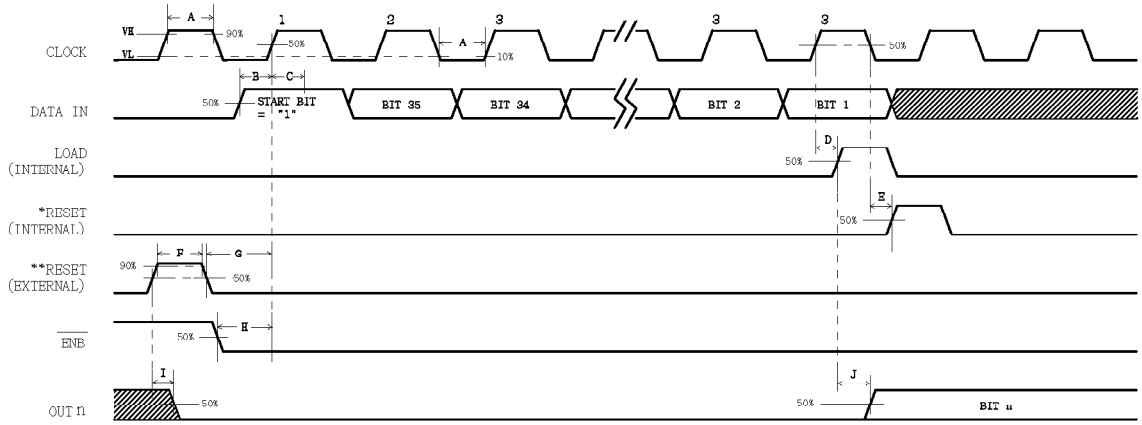
VDD=+5V, Ta=+25°C, UNLESS OTHERWISE SPECIFIED					
PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply,VDD		3.5	–	10	V
Power Supply Current	VDD=5V, excluding output	–	–	5	mA
Logic Input Voltages,VIH	VDD=5V	0.8VDD	VDD	VDD+0.3	V
VIL	VDD=5V	VSS-0.3	VSS	0.2VDD	V
Brightness Input,IBC		0	–	550	μA
Brightness Input Voltage	Input Current,IBC=550μA	3.0	3.2	4.0	V
Output Current, IOUT(OFF)	VOUT=3.0V	–	–	<0.5	μA
Output Current, IOUT(ON)	VOUT=1.0V	0	–	22	mA
	Brightness Input=0μA	0	–	<0.5	μA
	Brightness Input=100μA	3.5	3.6	3.7	mA
	Brightness Input=550μA	20	21	22	mA
Output Matching		–	–	5	%
Clock Input Frequency, FCLK		–	500K	2M	Hz

NOTE 1 : Output matching is calculated as the percent variation of each IOUT(ON)

to IOUT(AVG), where $I_{OUT(AVG)} = \{\sum_{n=1}^{35} I_{OUT(ON)}[BITn]\} \div 35$

■ TIMING CHART AND TIMING CONDITIONS

—— TIMING CHART



* THE INTERNAL RESET ONLY CLEARS ALL INTERNAL SHIFT REGISTERS.

** THE EXTERNAL RESET CLEARS ALL INTERNAL SHIFT REGISTERS AND LATCHES.

— TIMING CONDITIONS

ITEM	DESCRIPTION	MIN	TYP	MAX	UNIT
A	Clock pulse width	250	–	–	nS
B	Serial data setup time	30	–	–	nS
C	Serial data hold time	30	–	–	nS
D	Time between clock activation & internal load pulse activation	35	–	–	nS
E	Time between clock falling & internal reset pulse activation	35	–	–	nS
F	External reset pulse duration	25	–	–	nS
G	External reset inactive setup time	120	–	–	nS
H	Data enable setup time	70	–	–	nS
I	Time between external reset activation & the output off	25	–	–	nS
J	Time between internal load activation & new output states arising	30	–	–	nS

■ TRUTH TABLE

EXTERNAL RESET	$\overline{ENB}$	CLK	SERIAL DATA IN	SHIFT REGISTER CONTENTS I35 I34 I33 · · · I2 I1 I0	INTERNAL LOAD	INTERNAL RESET	LATCH CONTENTS I35 I34 I33 · · · I2 I1
L OR F	L OR F	↓	H	H R35 R34 · · · R3 R2 L	L	L	NO CHANGE
		↓	L	L R35 R34 · · · R3 R2 L	L	L	NO CHANGE
		↓	X	R35 R34 R33 · · · R2 R1 L	L	L	NO CHANGE
L OR F	L OR F	(1) (3) ↓↑↓ (2)	(1) X	P35 P34 P33 · · · P2 P1 H	H	L	P35 P34 P33 · · · P2 P1
			(2) X	L L L · · · L L L	L	H	P35 P34 P33 · · · P2 P1
			(3) H	H L L · · · L L L	L	L	P35 P34 P33 · · · P2 P1
			(3) L	L L L · · · L L L	L	L	P35 P34 P33 · · · P2 P1
L OR F	H	↓	X	L R35 R34 · · · R3 R2 L	L	L	NO CHANGE
		↓	X	R35 R34 R33 · · · R3 R2 L	L	L	NO CHANGE
L OR F	H	(1) (3) ↓↑↓ (2)	(1) X	P35 P34 P33 · · · P2 P1 H	H	L	P35 P34 P33 · · · P2 P1
			(2) X	L L L · · · L L L	L	H	P35 P34 P33 · · · P2 P1
			(3) X	L L L · · · L L L	L	L	P35 P34 P33 · · · P2 P1
H	X	X	X	L L L · · · L L L	L	L	L L L · · · L L

H = HIGH LOGIC LEVEL R = PREVIOUS STATE X = IRRELEVANT
L = LOW LOGIC LEVEL P = PRESENT STATE F = FLOATING

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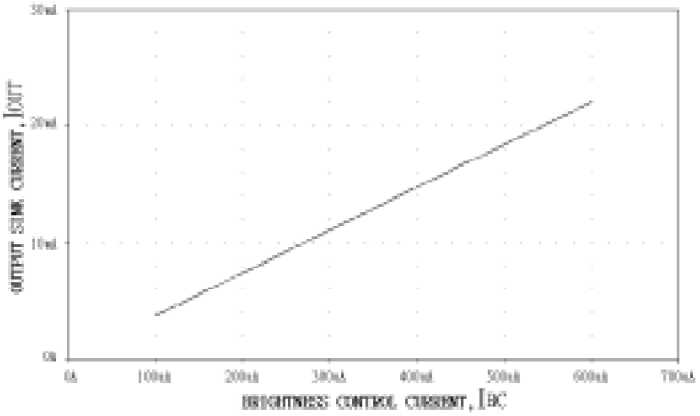
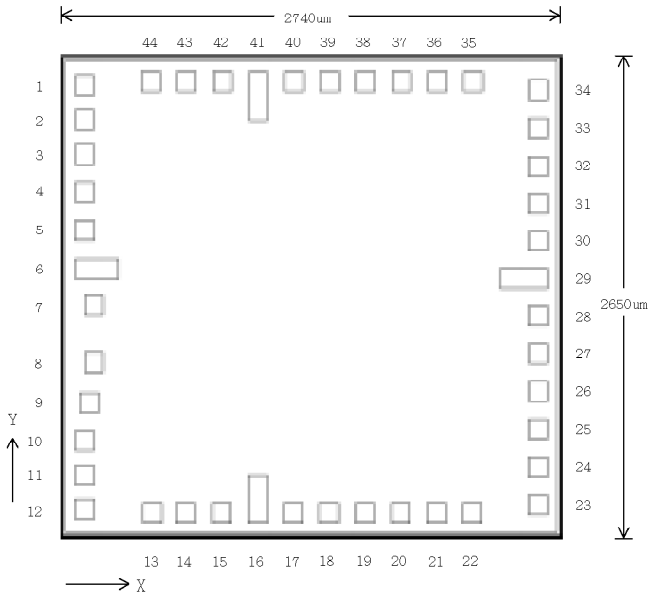
■ TYPICAL CHARACTERISTIC CURVES (VDD=5V，VOUT=1V)



■ PAD LOCATIONS AND PAD SIZE



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COORDINATES REFERENCE TO CENTER OF PAD AND PAD SIZE / ORIGION (0,0) AT CENTER OF PAD#12									
Pad No.	Name	X	Y	Pad Size	Pad No.	Name	X	Y	Pad Size
1	OUT3	0	+2168	95X BY 95Y	23	OUT23	+2411	0	95X BY 95Y
2	OUT2	0	+1988		24	OUT22	+2411	+193	
3	OUT1	0	+1809		25	OUT21	+2411	+386	
4	RESET	0	+1621		26	OUT20	+2411	+580	
5	B.C.	0	+1413		27	OUT19	+2411	+771	
6	VDD	+55	+1220	200X BY 95Y	28	OUT18	+2411	+965	
7	CLK	+49	+1036	95X BY 95Y	29	VSS	+2340	+1171	235X BY 95Y
8	DATA IN	+49	+728		30	OUT17	+2411	+1378	95X BY 95Y
9	$\overline{ENB}$	+25	+539		31	OUT16	+2411	+1571	
10	OUT35	0	+348		32	OUT15	+2411	+1764	
11	OUT34	0	+174		33	OUT14	+2411	+1957	
12	OUT33	0	0		34	OUT13	+2411	+2150	
13	OUT32	+404	−27		35	OUT12	+2008	+2194	
14	OUT31	+583	−27		36	OUT11	+1830	+2194	
15	OUT30	+762	−27		37	OUT10	+1650	+2194	
16	VSS	+938	+45	95X BY 235Y	38	OUT9	+1471	+2194	
17	OUT29	+1114	−27	95X BY 95Y	39	OUT8	+1292	+2194	
18	OUT28	+1292	−27		40	OUT7	+1113	+2194	
19	OUT27	+1472	−27		41	VSS	+938	+2121	95X BY 235Y
20	OUT26	+1651	−27		42	OUT6	+762	+2194	95X BY 95Y
21	OUT25	+1830	−27		43	OUT5	+583	+2194	
22	OUT24	+2009	−27		44	OUT4	+403	+2194	

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